ANALOG DEVICES

AN-320B
APPLICATION NOTE

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CMOS DACs and Op Amps Combine to Build Programmable Gain Amplifiers Part II

by John Wynne

This Application Note investigates the performance of dual CMOS DACs as gain determining elements in a PGA system. It details how greater accuracy over a wider dynamic range can be achieved with a dual DAC circuit as opposed to a single DAC solution. A dual DAC approach spreads the required system gain over two stages. This results in an overall system gain which is the product of the individual gain stages, but the overall gain error is essentially only the sum of the individual gain error terms.

Part I of this Application Note[1] looked at the error sources which exist when a CMOS DAC is used as a programmable resistance in the feedback loop of an op amp. A detailed comparison was also made between the performance of a PGA circuit based on a 14-bit DAC, the AD7534, (AD7538) and a 12-bit DAC, the AD7545.

DUAL DAC SOLUTION

With two DACs available in a single package – and, of course, two op amps also available in a single package – it becomes possible to use two simple PGA circuits in series without taking up too much extra printed circuit board area over that required by a single PGA stage. Figure 1 shows such a circuit. Each section contributes its own gain errors and offset errors to the overall error. Gain errors are due to DAC integral nonlinearity and to DAC gain error. Offset errors are due to DAC leakage currents and op amp input bias currents and input offset voltages.

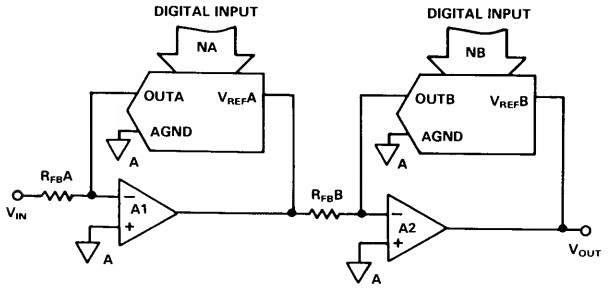

Figure 1. Dual DAC PGA Circuit

The dual DAC circuit does however exaggerate the dc offset error terms. The offset errors of the first stage are multiplied by the gain setting of the second stage. This can lead to quite large dc offset voltages for large gain settings, one third of a volt or more, at the output of the second stage. For this reason, dual DAC PGA systems are only considered suitable for ac signals, and the analysis presented here emphasizes this.

Since DAC gain error can be trimmed to zero (whereas nothing can be done to reduce the integral nonlinearity) it is instructive to first consider both the system gain and the percentage gain error due to DAC nonlinearity alone and then to add the DAC gain error terms. Following this, comparisons are made between the dual DAC performance and the performance of both the single 12-bit and 14-bit DAC systems which were the subject of Part I of this Application Note.

THE BASIC EQUATIONS FOR A DUAL DAC PGA

When only linearity errors are considered, the gain of a single stage is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{2^n}{(N+x)} \qquad (1)$$

Where n is the resolution of the DAC
x is the DAC linearity error in LSBs
and N is the DAC code in decimal.

With two similar stages in series the system gain is obviously:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{2^n}{N_A+X_A}\right) \cdot \left(\frac{2^n}{N_B+X_B}\right) \qquad (2)$$

Where A and B suffixes refer to DAC A (1st stage) and DAC B (2nd stage) respectively.

The percentage gain error of a single stage, again assuming zero DAC gain error, can be expressed as:

$$E(\%) = -\left(\frac{X}{N+X}\right) \cdot 100\% \qquad (3)$$

With two stages in series the overall gain error can generally be taken as the sum of both stages. If the first stage has a percentage gain error of E_A% and the second stage has E_B%, then the total system gain error can be expressed as:

$$\text{Error}(\%) = \left(E_A + E_B + \frac{E_A \cdot E_B}{100}\right)\% \quad (4)$$

For precision PGA systems these individual gain error terms, E_A and E_B, will normally be held to 1% or less. Under these conditions Equation 4 simplifies to:

$$\text{Error}(\%) = (E_A + E_B)\% \quad (5)$$

or using Equation 3:

$$\text{Error}(\%) = -\left(\frac{X_A}{N_A+X_A} + \frac{X_B}{N_B+X_B}\right) \cdot 100\% \quad (6)$$

Equation 2 shows the overall system gain is the product of the individual gain stages, while Equation 6 shows the overall percentage gain error is effectively the sum of the individual gain error terms. Hence, greater accuracy over a wider dynamic range is possible with a dual DAC PGA system over any single DAC solution. Also from Equation 2 the only constraint on the codes to both DACs, N_A and N_B, is that the overall system gain is achieved. Equation 6, however, indicates that in order to keep the gain error as small as possible, the codes to both DACs must be chosen to be as equal to each other as possible. Simultaneously meeting both these requirements results in the optimum system.

Equation 3, which gives the percentage gain error of a single stage, is correct for all gain settings except unity when an additional term must be added to the simple equation. This additional error term is due to an LSB worth of signal current being "lost" in the R-2R ladder termination resistor thereby making an ideal X1 gain impossible.

Therefore, for each DAC with a gain setting of unity (all 1s setting) an error term equal to 1LSB (expressed as a percentage) must be added to the total error term. For a dual-DAC system Equation (6) applies for all combinations of gain settings except those cases where an individual gain stage is set to unity gain. An extra error term must be added for each unity gain setting.

When both linearity errors and DAC gain errors are included, the gain of a single stage is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{2^n}{(N+X)(1+\Delta)} \quad (7)$$

$$\text{where } (1+\Delta) = \frac{R_{FB}}{R_{DAC}}$$

With two similar stages in series, the system gain is simply the product of the two stage gains or:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{2^n}{(N_A+X_A)(1+\Delta_A)}\right) \cdot \left(\frac{2^n}{(N_B+X_B)(1+\Delta_B)}\right) \quad (8)$$

For an individual stage the percentage gain error is:

$$\text{Error}(\%) = -\left\{\frac{\Delta}{(1+\Delta)} + \frac{1}{(1+\Delta)}\left(\frac{X}{N+X}\right)\right\} \cdot 100\% \quad (9)$$

Using similar reasoning to that used before in conjunction with Equations 4 and 5, the overall percentage gain error is again the sum of the individual error terms or:

$$\text{Error}(\%) = -\left[\left\{\frac{\Delta_A}{(1+\Delta_A)} + \frac{1}{(1+\Delta_A)}\left(\frac{X_A}{N_A+X_A}\right)\right\} + \left\{\frac{\Delta_B}{(1+\Delta_B)} + \frac{1}{(1+\Delta_B)}\left(\frac{X_B}{N_B+X_B}\right)\right\}\right] \cdot 100\% \quad (10)$$

Again, Equation 10 is valid for all combinations of gain settings except those cases where an individual gain stage is set to unity gain. For each unity gain setting an additional 1LSB (expressed as a percentage) must be added to the output error term.

COMPARING THE ERRORS

It is interesting to compare the dual DAC performance with both single 12-bit and 14-bit DACs on the basis of DAC nonlinearity alone and then to add the DAC gain error terms. Table A1 in Appendix 1 shows computed values of equation 6 at selected combinations of gain settings. The effect of DAC gain error is included in Table A2 which shows computed values of Equation 10. Also included in the tables are the individual codes for each DAC at the selected gain settings. The error terms in both tables are calculated for a PGA system based on the AD7547LN. This is a dual 12-bit DAC with full parallel loading, housed in a skinny 24-pin package. Relevant specifications for this device are shown in Table I. The gain error analysis leading to Equations 6 and 10 assumed that the individual loop gains of the dual DAC system were sufficiently high so as to cause no appreciable error. This is a valid assumption at dc and low frequencies since extreme gain settings are not used in practice. This topic is dealt with later in greater detail.

Parameter	AD7547LN $T_A = +25°C$	AD7547LN $T_A = +70°C$	AD7547UQ $T_A = +125°C$
Resolution, n	12 bits	12 bits	12 bits
Relative Accuracy, X (Integral Linearity)	±1/2LSB max	±1/2LSB max	±1/2LSB max
Gain Error	±1LSB max	±1LSB max	±2LSB max
Output Leakage, I_{LKG}	10nA max	150nA max	250nA max
Input Resistance	20kΩ max	20kΩ max	20kΩ max

NOTE: $V_{DD} = +12V$ to $+15V$

Table I. AD7547 Dual DAC Specifications at $T_A = +25°C$, $+70°C$ and $+125°C$

Figure 2 plots the results due solely to DAC nonlinearity errors of the three PGA circuits under comparison. As might have been expected, the dual DAC circuit produces the highest errors at the lowest gains. For system gains of 1 to 4 the dual 12-bit DAC circuit produces the highest errors. At a gain of 4, however, its performance equals

that of a single 12-bit DAC circuit and thereafter is increasingly superior with increasing gain. At a gain of 64 its performance equals that of a single 14-bit DAC circuit, and thereafter is increasingly superior with increasing gain. The straight line representation in Figure 2 of percentage error versus gain for the dual DAC circuit, however, is an idealization. Because the total gain error now depends on two DAC codes, a number of code combinations exist which will give the same gain (within some chosen tolerance) but produce widely different system gain errors. For instance, if the required gain is 64, the obvious and best distribution of gain settings for the dual DAC system is X8 and X8. From Figure 2 this will give a system error of approximately ±0.2%. If gain settings of X1 & X64 were

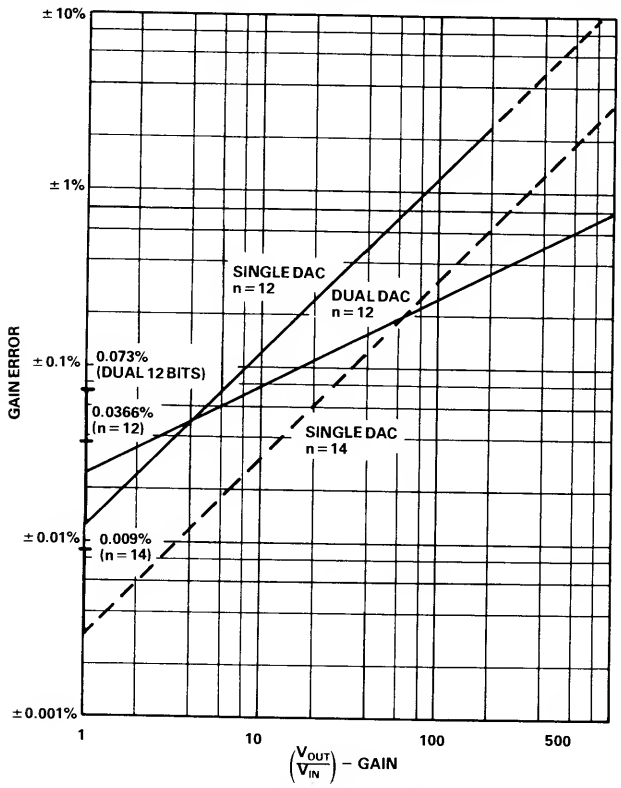

Figure 2. Comparison of Worst Case Gain Errors between PGA Systems Based on Single and Dual 12-Bit Resolution, 12-Bit Accurate DACs and a 14-Bit Resolution, 14-Bit Accurate DAC. DAC Gain Error Is Zero in All Cases

chosen, the system error would be slightly greater than ±0.8%, a four-fold increase. For this example the optimum codes are obvious. However, for many other system gains which are not integer powers of two and which may not even be integers, choosing the optimum gain distribution will require some attention.

The total error results of Table A2 are plotted in Figure 3 along with results from Part I of this Application Note, of a single 12-bit DAC (AD7545LN) and a single 14-bit DAC (AD7534KN). The very tight gain error of the dual DAC results in a system where the gain error, at all gain settings, can actually be less than that of a single 12-bit DAC.

DYNAMIC PROBLEMS
STABILITY AND COMPENSATION

For the purposes of investigating the dynamic performance of DAC-based PGA systems, an equivalent circuit for a single DAC and op amp stage is shown in Figure 4. Programmable circuit gain is ideally set by resistors R_{FB} and R_{EQ} around the op amp. A real DAC, however, also adds both a code dependent resistance R_O and code dependent capacitance C_O between the op amp summing junction and ground. Capacitance C_2 represents the sum of both stray capacitance and any added capacitance across the equivalent feedback resistor. Since this equivalent resistance can normally be quite large, the effect of C_2 on the frequency response can be very important.

With an internally compensated op amp, whose open loop gain rolls off due to a single dominant pole, the 3dB bandwidth for an ideal PGA system is very easily found from the constant gain-bandwidth product concept. For instance, if the gain-bandwidth product of A1 in Figure 4 is 1.10^6, then for a X1 inverting gain ($1/\beta = 2$), the ideal closed-loop bandwidth is 500kHz; whereas, for a X64 gain, it is reduced to approximately 15kHz. Thus, signal bandwidth is inversely proportional to gain.

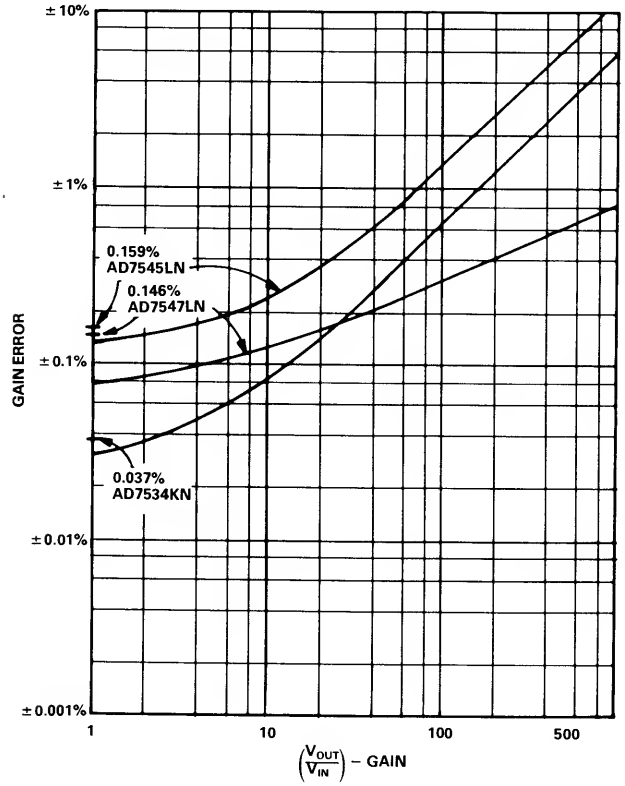

Figure 3. Comparison of Theoretical Worst Case Gain Errors between the Three PGA Systems when DAC Gain Errors Are Included

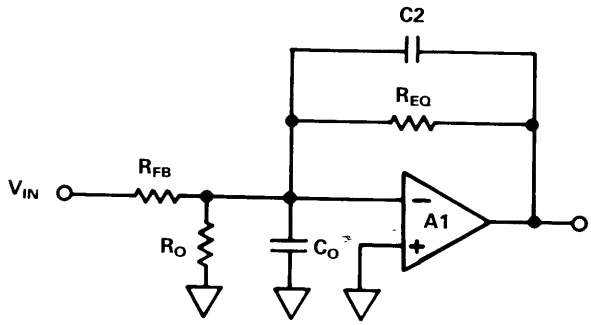

Figure 4. Equivalent Circuit for a Single Stage

The output capacitance of the DAC, C_0, combines with R_{EQ} to add an extra pole to the closed-loop response. This pole upsets the unconditional stability characterized by a loop gain slope of −6dB/octave and a −90° maximum phase shift by adding extra phase shift. The amount of extra phase added depends on the position of the spurious pole with respect to the undisturbed unity loop gain frequency. If the phase margin is reduced by too much, the system stability is upset and gain peaking becomes increasingly evident. For a PGA system intended to amplify ac signals, gain peaking can be a serious source of error. Loop stability margins can be restored and gain peaking eliminated by placing a phase lead capacitor C_2 across the feedback resistor R_{EQ}.

The value of C_2 plays an important part in the system performance. If C_2 is too small (with respect to C_0), gain peaking may occur. If it is too large, the bandwidth of the amplifier will be unnecessarily reduced. Ideally, the ratio of C_0 to lead capacitance C_2 should be equal to the closed-loop gain minus one. For a fixed gain setting it is possible to satisfy this requirement. However, with every new gain setting, the optimum value for C_2 will change. In practice, the best solution is to choose a value for C_2 which avoids gain peaking at the gain setting most liable to exhibit it – the X1 gain setting. For the circuit of Figure 4, the closed-loop gain can be expressed as:

$$\frac{1}{\beta} = \frac{\left\{1+R_{EQ}\left(\frac{1}{R_{FB}}+\frac{1}{R_0}\right)\right\}\left\{1+S\,(C_0+C_2)R\right\}}{1+SC_2R_{EQ}} \qquad (11)$$

At low frequencies the closed-loop gain is equal to the dc noise gain, G_N, of the circuit:

$$G_N = 1 + R_{EQ}\left(\frac{1}{R_{FB}}+\frac{1}{R_0}\right) \qquad (12)$$

At the X1 gain setting, R_{EQ} is approximately equal to R_{FB} and $R_0 = 3\ R_{FB}$ (for the AD7547). Using these values in Equation 12 the ideal C_0/C_2 ratio is found from:

$$\frac{C_0}{C_2} = G_N - 1 = \frac{1}{\beta} - 1$$

$$\text{or } C_2 = 0.75\,C_0 \qquad (13)$$

At gain settings other than unity the value of C_2 is larger than necessary to ensure no gain peaking occurs. The drawback to this is that the overall bandwidth is reduced and the settling time is increased.

SMALL-SIGNAL BANDWIDTH

For Figure 4, the output signal voltage can be expressed as:

$$V_{OUT} = -V_{IN} \cdot \frac{R_{EQ}}{R_{FB}}\left(\frac{1}{(1+SC_2\,R_{EQ})}\right) X\left[\frac{1}{1+\frac{1}{A(\omega)}\left\{\frac{G_N\,(1+S\,(C_0+C_2)R)}{1+SC_2\,R_{EQ}}\right\}}\right] \qquad (14)$$

where $R = R_{FB} \| R_0 \| R_{EQ}$

and $A(\omega)$ is the open-loop gain of the amplifier, a complex quantity.

The closed-loop signal bandwidth is set at $1/2\pi\ C_2\ R_{EQ}$, by the value chosen for C_2. In terms of the digital input code to the DAC the 3dB signal bandwidth can be expressed as:

$$f_{3dB} = \frac{D}{2\pi C_2\,RLAD} \qquad (15)$$

and since system gain is inversely proportional to D:

$$f_{3dB} = \frac{1}{GAIN} \cdot \left(\frac{1}{2\pi C_2\,RLAD}\right) \qquad (16)$$

When two stages are cascaded the overall bandwidth is:

$$1.1\sqrt{\left(\frac{0.35}{f_{3dBA}}\right)^2+\left(\frac{0.35}{f_{3dBB}}\right)^2} \qquad (17)$$

where f_{3dBA} and f_{3dBB} are the high frequency 3dB cutoffs for the two stages. If n stages have the same cutoff frequency, f_{3dB}, the cascaded bandwidth is:

$$\sqrt{2^{1/n}-1} \cdot f_{3dB} \qquad (18)$$

For two stages, the cascaded bandwidth is $0.64\ f_{3dB}$. In a cascaded system, the widest overall bandwidth is achieved when each stage has the same high frequency 3dB cutoff. This is equivalent to saying that the widest overall bandwidth occurs when each stage has the same gain setting. This statement complements that which was previously made in relation to Equation 6 viz. that in order to keep the gain error as small as possible the codes to both DACs must be chosen to be as equal to each other as possible.

DYNAMIC GAIN ERRORS

At the cascaded 3dB cutoff frequency, the magnitude of the output signal is 0.707 times the input signal – approximately 30% down. In certain applications this amount of gain error could be excessive. In these instances the useable bandwidth should be considered in terms of the additional gain error resulting from the fall-off in closed-loop signal gains. The reduced bandwidth for the cascaded system is determined by the gain equation:

$$\text{Amplitude} = \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^2} \qquad (19)$$

Both stages are assumed to have the same high frequency 3dB cutoff. For example, the reduced bandwidth necessary to restrict additional gain errors to below 0.1% or the total amplitude to 0.999, can be found from Equation 19 to be:

$$f = 0.032\,f_{3dB}$$

$$\text{or } f = 0.032 \cdot (f_{CASC}/0.64)$$

$$= 1/20^{th} \text{ of } f_{CASC} \qquad (20)$$

This means that signal frequencies up to 1/20 of the cascaded bandwidth will have less than 0.1% of additional gain error.

Finite loop gain can also contribute additional gain error. The square bracketed term in Equation 14 is called the gain error factor. Ideally this factor is equal to unity; the amount by which it differs from unity is equivalent to the additional gain error due to finite loop gain. Appendix 2 contains both an analysis of the gain error factor and a worked example of its magnitude in a typical application. In comparison with the gain errors introduced by the signal bandwidth, the analysis indicates that additional gain errors due to finite loop gain can be ignored.

NOISE AND DISTORTION

Noise does not cause gain errors in the sense of introducing constant multiplicative terms. Rather, it acts to reduce the signal to distortion ratio of the PGA system. This topic is well covered by standard op amp texts and will not be discussed here. Analog Devices' CMOS DACs are manufactured with high quality, thin-film resistors and exhibit very little excess noise over that expected from an equivalent Johnson noise source. In addition, since these thin-film resistors have a very small voltage coefficient, any distortion through the R-2R ladder results from R_{ON} modulation of the signal-steering switches. In practice, however, distortion is usually limited by the op amp itself.

AC COUPLING THE OUTPUT

In a dual DAC PGA system the dc offset errors of the first stage are multiplied by the gain of the second stage. This can lead to quite large dc error voltages at the second stage output. AC coupling the output of the second stage obviously eliminates the problem but adds a low frequency pole to the response. This low frequency pole will contribute gain errors to low frequency input signals. The situation is exactly analogous to the gain error caused by high frequency fall-off discussed previously. Placing the ac coupling capacitor after the second stage also allows a single trim potentiometer to correct for DAC gain errors of both DACs. However, the temperature coefficient of the trim potentiometer will not match the temperature coefficient of the thin-film resistors of the DACs resulting in a change in DAC gain error over temperature. Taking into account the fact that the DAC gain error of the AD7547LN is specified to remain within ±1LSB from 0 to +70°C, better circuit performance over temperature may result if no trim potentiometer is used.

TEST RESULTS

AC measurements for a PGA system based on an AD7547LN dual-DAC and two AD OP-27E op amps are plotted in Figure 5. The "starred" points indicate the measured errors at the selected gain settings between X1 and X512. At each gain setting the input signal level was adjusted to provide a 6V rms output signal level. The test frequency was 200Hz. As a comparison, the worst-case theoretical curves from Figures 2 and 3 for a dual DAC PGA system area also included in Figure 5. As mentioned previously in the text, these solid-line curves are in fact idealizations since in a dual DAC system any desired gain can usually be realized by different code combinations.

Parameter	AD OP-27E $T_A = +25°C$	AD OP-27E $T_A = +70°C$	AD OP-27A $T_A = +125°C$
Open-Loop Gain, A_{OL}	1.10^6 min	$0.75.10^6$ min	$0.6.10^6$ min
Input Bias Current, I_B (–)	40nA max	60nA max	60nA max
Input Offset Voltage, V_{OS}	25μV max	50μV max	60μV max

NOTE: $V_{DD} = +15V, V_{SS} = -15V$

Table II. AD OP-27 Specifications at $T_A = +25°C$, +70°C and +125°C

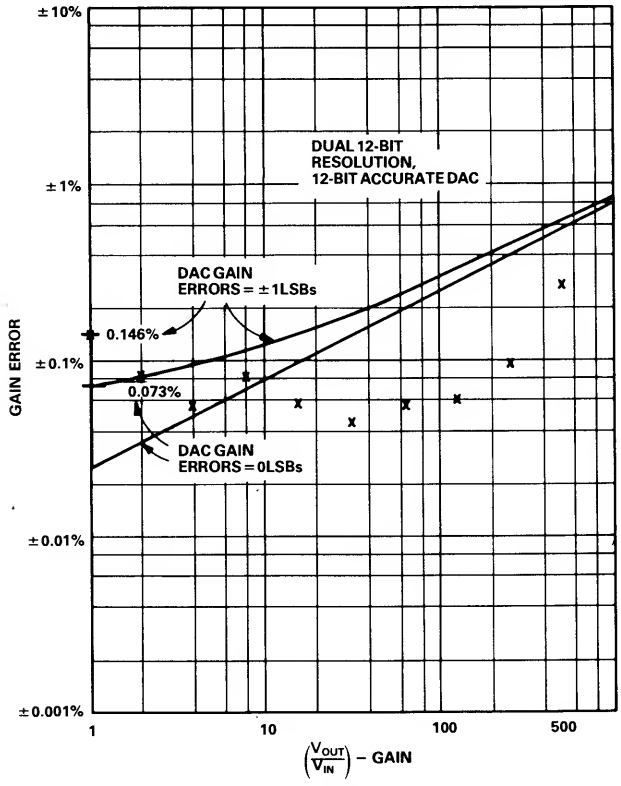

Figure 5. Measured vs. Theoretical Worst Case Gain Errors for AD7547-Based System

Output voltage settling time was measured for a step input change at two fixed gain settings (X1, X64). The output response is shown in the photographs of Figure 6a and 6b. For Figure 6a (X1 Gain) the input step size is ±200mV, and for Figure 6b (X64 Gain) it is ±154mV. The input signal rise and fall time in either case from the 10% to 90% points was 400ns.

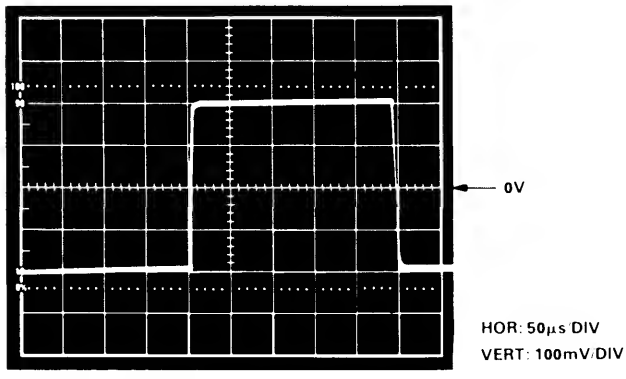

Figure 6a. Gain of 1. Output Response to ±200mV Step Input, AD7547 System

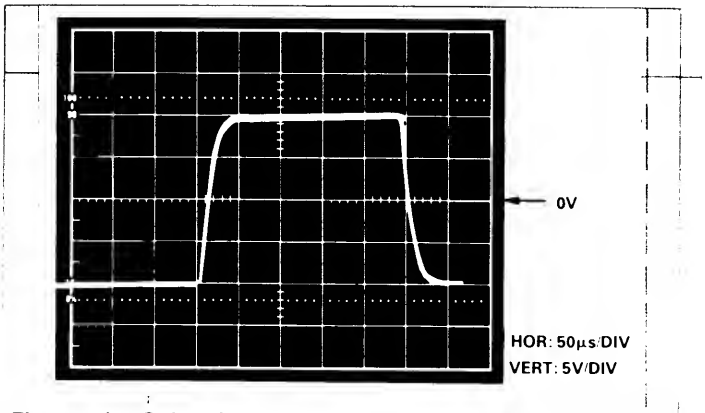

Figure 6b. Gain of 64. Output Response to ±154mV Step Input, AD7547 System

Settling time to within ±0.01% for the X1 case is less than 15μs; whereas, settling time for the X64 case is less than 100μs. Output voltage settling time was also measured for a change in gain settings with a steady input signal. Figure 6c shows the output response when changing from a X1 setting to a X64 setting. To get this photograph the codes in both DACs are simultaneously switched between 4095_{10} (X1 and X1) and 512_{10} (X8 and X8). The input loading structure of the AD7547 allows simultaneous updating of the DAC registers with common data. The output voltage settling time to within ±0.01% is less than 70μs going from X1 to X64, while going from X64 to X1 it is less than 15μs. The effect of the high-speed, wide bandwidth AD OP-27 op amps on voltage settling time is obvious from a comparison of these photographs with those of Figure 8 in Part I of this Application Note.

Total harmonic distortion levels versus gain settings are shown in the right hand column of Table III. For comparison, the harmonic distortion levels measured previously for the AD7545 – and AD7534 – based PGAs are also included in this table. In all three cases, for any particular gain setting, the input signal level was adjusted to provide a 6V rms output signal level. The test frequency was 200Hz. The bandwidth of the Hewlett Packard HP339A distortion measuring set on which the measurements were taken was purposely limited by the set's 3rd order, 30kHz low pass filter to minimize the noise bandwidth.

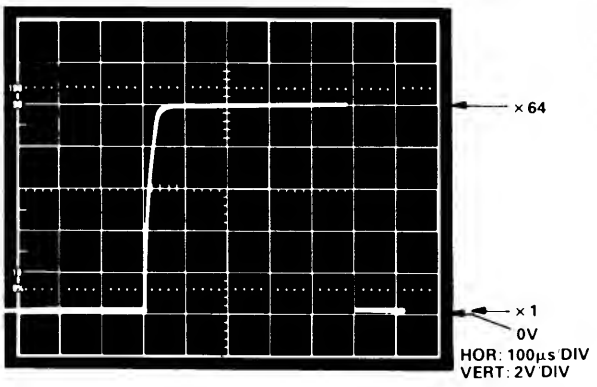

Figure 6c. Output Response when Gain Switching between X1 and X64. Constant Input Signal of + 154mV, AD7547 System.

GAIN	AD7545LN & AD OP-07	AD7534LN & AD OP-07	AD7547LN & AD OP-27 (2)
X 1	<−90dB	<−90dB	<−90dB
X 2	<−90dB	<−90dB	<−90dB
X 4	<−90dB	<−90dB	<−90dB
X 8	−89dB	−88dB	<−90dB
X 16	−86dB	−86dB	<−90dB
X 32	−82dB	−83dB	<−89dB
X 64	−76dB	−79dB	<−84dB
X 128	Not Measured	Not Measured	<−79dB
X 256	Not Measured	Not Measured	<−74dB
X 512	Not Measured	Not Measured	<−68dB

Table III. Total Harmonic Distortion Levels vs. Gain Settings for a Constant 6V rms Output Signal

The small signal bandwidth at a number of gain settings is shown in Table IV. These measured frequencies follow closely the values predicted from Equations 15 – 18. A value of 47pF was used for the phase lead capacitor, C2, in each of the two stages. With large signal levels and high signal frequencies distortion becomes severe due to op-amp limitations. For example, for the AD OP-27 with an output signal level of 6V RMS the limit before distortion rapidly increases is typically 40kHz. The input signal levels used for the bandwidth measurements were varied with gain setting in order to maintain total harmonic distortion below 75dB. Thus at high gain settings (small bandwidths), signal levels were high in order to maximize the signal-to-noise ratio; at low gain settings (wide bandwidths), signal levels were low in order to avoid op amp induced distortion.

System Gain	F_{CASC} Measured	F_{CASC} Computed
X 1	135kHz	135.5kHz
X 4	60kHz	67.7kHz
X 8	44kHz	43kHz
X 16	32kHz	34kHz
X 64	15.4kHz	16.9kHz
X 256	7.8kHz	8.4kHz

Table IV. Small Signal Bandwidth vs. Gain Setting for Dual-DAC PGA System

Table V compares the voltage noise performances of the AD7547-based PGA and the single DAC-based systems.

GAIN	AD7545LN & AD OP-27	AD7534KN & AD OP-27	AD7547LN & AD OP-27
X 1	5.5μV	4.5μV	6.2μV
X 2	9μV	7μV	11.2μV
X 4	18μV	12μV	17μV
X 8	35μV	23μV	31.5μV
X 16	72μV	45μV	63μV
X 32	145μV	89μV	127μV
X 64	285μV	175μV	260μV

Table V. Output Voltage Noise vs. Gain Settings. Readings are rms, 22Hz to 22kHz.

To help the comparison the same AD OP-27E op amp was used in both of the single DAC circuits and in the first stage of the dual DAC circuit. No phase lead compensation capacitors were used in any of the circuits. The results indicate that there is little difference between the single 12-bit and dual 12-bit PGAs in terms of output voltage noise.

FIXED GAIN CIRCUIT

In addition to programmable gain in a system, a certain amount of fixed gain can also be useful. It is possible to combine both functions around a single DAC plus op amp. The circuit is shown in Figure 7. Resistors R1 and R2 determine the fixed amount of gain. Normally, the DAC input resistance would be included in the gain expression making circuit gain a function of that resistance. This problem is eliminated (Reference 2) by adding an input resistor in series with R_{FB}. This input resistor, R_{IN}, has a value equal to the parallel combination of R1 and R2. The output voltage is:

$$V_{OUT} = -\frac{V_{IN}}{D} \cdot \left(1+\frac{R1}{R2}\right) \quad (21)$$

Resistors R1, R2 and R_{IN} should have similar temperature coefficients, but they need not match the temperature coefficient of the DAC. Minor gain adjustments can be made by varying the attenuator ratio as adjustment sensitivity is almost unaffected by R1.

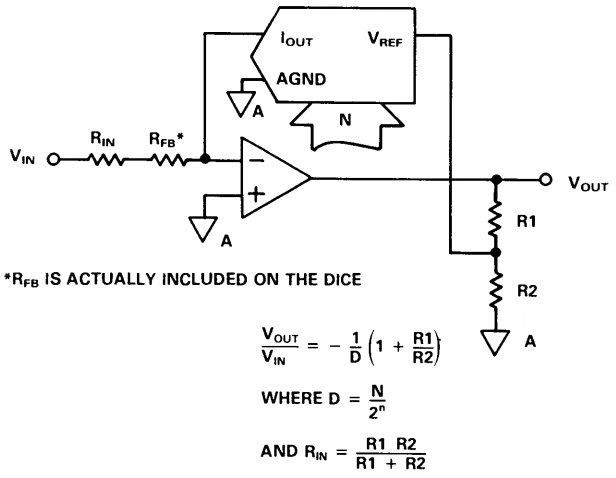

Figure 7. Adding Some Fixed Gain to the Basic Stage

REFERENCES

1. "CMOS DACs and Op Amps Combine to Build Programmable Gain Amplifiers, Part I" by John Wynne. Available from Analog Devices, Publication No. E1037-15-1/87.
2. "Input Resistor Stabilizes MDAC's Gain" by Paul Brokaw, EDN, January 7, 1981, pp. 210-211.
3. Transaction Brief; "Expression for the Output Resistance of a Switched R-2R Ladder Network" by E. David Erb and Gregory M. Wierzba. IEEE Trans. Circuits & Systems, Vol. CAS-30, No. 3, March 1983, pp. 167-169.

APPENDIX 1

	1st STAGE		2nd STAGE		
GAIN	DAC A Code N_A (Decimal)	Worst Case Error, E_A	DAC B Code N_B (Decimal)	Worst Case Error, E_B	Total Error $E_A + E_B$
1	4095	+0.0366%	4095	+0.0366%	+0.0732%
2	2896	+0.0173%	2896	+0.0173%	+0.0345%
3	2365	+0.0211%	2365	+0.0211%	+0.0423%
4	2048	+0.0244%	2048	+0.0244%	+0.0488%
8	1024	+0.0489%	2048	+0.0244%	+0.0733%
16	1024	+0.0489%	1024	+0.0489%	+0.0978%
32	512	+0.0978%	1024	+0.0489%	+0.1467%
64	512	+0.0978%	512	+0.0978%	+0.1956%
128	256	+0.196 %	512	+0.0978%	+0.294 %
256	256	+0.196 %	256	+0.196 %	+0.392 %
512	128	+0.392 %	256	+0.196 %	+0.588 %

$$\text{Error}(\%) = -\left\{\frac{XA}{NA+XA} + \frac{XB}{NB+XB}\right\} \cdot 100\% \qquad (6)$$

Table A1. Computed Worst Case Gain Error for Equation 6 for Dual 12-Bit Resolution (n = 12), 12-Bit Accurate (X = ±0.5LSBs) DACs with Zero DAC Gain Error. The Unity Gain Values Include Additional Error Terms as Discussed in the Text.

	1st STAGE		2nd STAGE		
System Gain	DAC A Code N_A (Decimal)	Worst Case Error, E_A	DAC B Code N_B (Decimal)	Worst Case Error, E_B	Total Error $E_A + E_B$
1	4095	+0.073 %	4095	+0.073 %	+0.0146%
2	2896	+0.0417%	2896	+0.0417%	+0.083 %
3	2365	+0.0456%	2365	+0.0456%	+0.091 %
4	2048	+0.049 %	2048	+0.049 %	+0.098 %
8	1024	+0.073 %	2048	+0.049 %	+0.122%
16	1024	+0.073 %	1024	+0.073 %	+0.146%
32	512	+0.122 %	1024	+0.073 %	+0.195 %
64	512	+0.122 %	512	+0.122 %	+0.244 %
128	256	+0.22 %	512	+0.122 %	+0.342 %
256	256	+0.22 %	256	+0.22 %	+0.44 %
512	128	+0.417 %	256	+0.22 %	+0.637 %

$$\text{Error}(\%) = -\left[\left\{\frac{\Delta_A}{(1+\Delta_A)} + \frac{1}{(1+\Delta_A)}\left(\frac{X_A}{N_A+X_A}\right)\right\} + \left\{\frac{\Delta_B}{(1+\Delta_B)} + \frac{1}{(1+\Delta_B)}\left(\frac{X_B}{N_B+X_B}\right)\right\}\right] \cdot 100\% \qquad (10)$$

Table A2. Computed Worst Case Gain Error for Equation 10 for Dual 12-Bit Resolution (n = 12), 12-Bit Accurate (X = ±0.5LSBs) DACs with DAC Gain Errors of ±1LSB (= ±1/4096). The Unity Gain Values Include Additional Error Terms as Discussed in the Text.

APPENDIX 2

The gain error factor from equation 14 is:

$$\frac{1}{1+\frac{1}{\beta A(\omega)}} = \frac{1}{1+\frac{1}{A(\omega)}\left\{\frac{G_N(1+S[C_0+C_2]R)}{1+S\,C_2\,R_{EQ}}\right\}} \quad \text{(A1)}$$

or

$$\frac{1}{1+\frac{1}{\beta A(\omega)}} = \frac{1}{1+\frac{1}{A(\omega)}\left\{\frac{G_N(1+j\,\omega/\omega_1)}{1+j\,\omega/\omega_2}\right\}} \quad \text{(A2)}$$

where $\omega_1 = \frac{1}{(C_0+C_2)\cdot R}$

and $\omega_2 = \frac{1}{C_2 \cdot R_{EQ}}$

Equation A2 can be rewritten emphasizing the phasor qualities of its terms:

$$\frac{1}{1+\frac{1}{\beta A(\omega)}} = \frac{1}{1+\left|\frac{G_N \cdot r_1}{A_{OL}(\omega)\cdot r_2}\right| \angle\theta} \quad \text{(A3)}$$

where $r_1 = \sqrt{1+(\omega/\omega_1)^2}$

$r_2 = \sqrt{1+(\omega/\omega_2)^2}$

$A_{OL}(\omega) = A_{OL}/\sqrt{1+(\omega/\omega_P)^2}$

A_{OL} is the dc value of the open loop gain and ω_P is the break frequency of the op amp

Also, $\angle\theta = \theta_1 - \theta_2 + \theta_3$ (A4)

where $\theta_1 = t_{an}{}^{-1}\left(\frac{\omega}{\omega_1}\right)$

$\theta_2 = t_{an}{}^{-1}\left(\frac{\omega}{\omega_1}\right)$

$\theta_3 = t_{an}{}^{-1}\left(\frac{\omega}{\omega_P}\right)$

The magnitude of the gain error factor can now be written as:

$$\left|\frac{1}{1+\frac{1}{\beta A(\omega)}}\right| = \frac{1}{\sqrt{1+\left|\frac{G_N\cdot r_1}{A_{OL}(\omega)\cdot r_2}\right|^2 + 2\cos\theta\left|\frac{G_N\cdot r_1}{A_{OL}(\omega)\cdot r_2}\right|}} \quad \text{(A5)}$$

Since the cosine of an angle θ between 90° and 180° is negative, then it is possible for the gain error factor of Equation A5 to be greater than unity causing gain peaking. From Equation A4 the angle θ is the sum of θ_3, due to the op amp pole at ω_P; θ_1 due to the closed-loop zero at ω_1 and θ_2, due to the closed-loop pole at ω_2. The relative positions of ω_1 and ω_2 determine the overall response of the system.

Equation A5 is the gain error factor for a single stage. For a dual DAC PGA the overall gain error factor can be taken to be the sum of both stage factors.

From the AD7547 data sheet, $C_0 = 140$pF max and $R_{LAD} = 20$kΩ max. The value of compensation capacitor, C_2, required to prevent gain peaking depends upon the minimum value of programmable gain to be used. For a X1 gain setting $C_2 = 0.75\ C_0$ or $C_2 = 100$pF (from Equation 13). If the overall gain required is X16, then the widest system bandwidth occurs when both stages have gain settings of X $\sqrt{16}$ i.e., X4. The signal bandwidth for a single stage is found from Equation 16 to be:

$$f_{3dB} = \frac{1}{GAIN}\left(\frac{1}{2\pi C_2 R_{LAD}}\right)$$

$$= 20\text{kHz}$$

The cascaded bandwidth is:

$$f_{CASC} = 0.64\, f_{3dB}$$

$$= 12.7\text{kHz}$$

If the additional gain error due to signal roll-off is to be kept below, say, 0.1%, then from Equation 19, the useable system bandwidth reduces to 1/20 of the cascaded bandwidth, i.e., 600Hz. If AD OP-27 op amps are used which have an open-loop gain of approximately 80dB at 600Hz, then, from Equation A5, the additional gain error due to a single stage is found to be less than 0.004%. Two similar stages will contribute less than 0.01% of additional gain error. This error is an order of magnitude below that caused by signal roll-off. Hence, in comparison with signal roll-off, nonideal gain error factors can be ignored as a source of additional gain error.

A value of 5.5 for G_N was used in Equation A5 to determine the additional gain error. Appendix 3 shows how this value was determined and gives a software listing to help determine G_N for any other gain setting.

APPENDIX 3

From Equation 12

$$G_N = 1 + R_{EQ}\left(\frac{1}{R_{FB}} + \frac{1}{R_O}\right)$$

This can be rewritten as

$$G_N = 1 + \frac{R_{EQ}}{R_{FB}}\left(1 + \frac{R_{FB}}{R_O}\right)$$

or $G_N = 1 + (\text{Stage Gain}) \cdot \left(1 + \frac{R_{FB}}{R_O}\right)$

Table A3 lists a program which solves the $(1 + R_{FB}/R_O)$ term for a straight R-2R ladder network. It is an extention of the expression contained in Reference 3. It is written for a HP85 computer. The resolution of the DAC is entered first followed by the code in decimal for which the output resistance is required. The answer, R_{OUT}, is equal to

$$R_{OUT} = 1 + \frac{R_{FB}}{R_O}$$

This is now used to find the noise gain, G_N.

```
  4 ! ************************
    **
  5 ! * PROGRAM TO PLOT DAC ROUT
     *
  6 ! * FOR ANY NUMBER OF BITS
     *
  7 ! ************************
    **
  8 CLEAR
 10 DISP "NO OF BITS" @ INPUT N
 15 DIM B(20)
 18 DISP @ DISP "ENTER CODE IN D
    EC"
 20 INPUT F
 25 D=F
 27 CLEAR @ DISP @ DISP @ DISP "
              COMPUTING"
 30 GOSUB 1000
 40 GOSUB 4000
 50 DISP @ DISP
 52 CLEAR @ DISP @ DISP @ DISP "
    NUMBER OF BITS = ";N
 54 DISP @ DISP @ DISP "CODE IN
    DEC = ";F
 56 DISP @ DISP
 60 DISP "ROUT = ";E
 70 END
1000 REM DEC TO BIN
1010 FOR C=N-1 TO 0 STEP -1
1020 D=D-2^C
1030 IF D<0 THEN D=D+2^C @ B(N-C
     )=0 ELSE B(N-C)=1
1040 NEXT C
1050 RETURN
4000 REM CALCULATE ROUT
4005 T=0 @ S=0
4010 FOR C=1 TO N STEP 1
4020 IF B(C)=1 THEN 4040
4030 GOTO 4070
4040 Y=1+2^(1-2*C)
4050 T=T+Y
4070 NEXT C
4080 FOR C=2 TO N-1
4090 FOR J=C+1 TO N
4100 IF B(C)=1 AND B(J)=1 THEN 4
     120
4110 GOTO 4140
4120 X=2^(2-C-J)*(2^(2*C-2)-1)
4130 S=S+X
4140 NEXT J
4150 NEXT C
4160 E=T-S @ E=3/E
4165 E=1/E
4170 E=E+1
4175 E=E-F/2^N
4190 RETURN
```

Table A3. HP-85 Listing for Solving $(1+R_{FB}/R_O)$ Ratio